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CLAIMS

What is claimed is:

1.   An multiplexed analog bus with a plurality of signal busses in parallel, wherein signals are selected onto the signal busses prior to being demultiplexed.

2.   The bus as set forth in claim 1 wherein the selected signals are allowed to pre-charge each bus prior to reading.

3.   The bus as set forth in claim 1 wherein the signals are selected in parallel along the column to pre-charge the busses prior to being demultiplexed.

4.   The bus as set forth in claim 1 wherein the bus has the signals either demultiplexed on a substrate or externally.

5.   The bus as set forth in claim 1 wherein the busses are multiplexed and demultiplexed in random or sequential order.

6.   The bus as set forth in claim 1 wherein the busses are selected at once.

7.   An imager comprising a differential video bus.

8.   The imager as set forth in claim 7 wherein a differential video contains a desired signal on one node and a common mode noise on both.

9.   The imager as set forth in claim 8 wherein the differential video contains different video signals on both nodes and common mode noise on both nodes.

10.   An imager comprising analog processing to subtract the common mode noise.

11.   An imager as set forth in claim 10 wherein analog bus can either be differential or single ended.

12.   A video bus with multiple signals selected at once in parallel.

13.   The bus as set forth in claim 12 wherein the video bus has multiple signals selected in sequence or in random.

14.   A column to column interpolation by selecting two or more columns on the same video bus.

15.   The column to column interpolation as set forth in claim 14, wherein the interpolation is performed by reading two or more signals separately and combined using the same video signals.

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16. A column to column interpolation by selecting two or more analog busses for demultiplexing at the same time.

17. The column to column interpolation as set forth in claim 16 wherein multiple signal busses are demultiplexed onto the same node.

18. The column to column interpolation as set forth in claim 16 wherein the demultiplexion is in sequence or random

19. A row to row interpolation by selecting two or more rows simultaneously to be combined along the column.

20. The row to row interpolation as set forth in claim 19 wherein the row to row interpolation for active column sensors is accomplished by selecting two or more rows simultaneously and having their currents combined along the column.

21. The row to row interpolation as set forth in claim 19 wherein multiple row selection are in sequence or in random.

22. An interpolation along both the rows and columns at the same time by selecting two adjacent rows and two adjacent columns.

23. The row to row interpolation as set forth in claim 22 wherein two or more row and column selections are in sequence or random.

24. A column to column binning by selecting two or more analog busses for demultiplexing at the same time.

25. The column to column binning as set forth in claim 24 wherein multiple signals busses are demultiplexed onto the same node.

26. The column to column binning as set forth in claim 24 wherein multiple signal busses are demultiplexed in sequence or random

27. A row to row binning by selecting two or more rows simultaneously to be combined along the column.

28. The row to row binning as set forth in claim 27 wherein the row to row binning for active column sensors is accomplished by selecting two or more rows simultaneously and having their currents combined along the column.

29. The row to row binning as set forth in claim 27 wherein multiple row selection are in sequence or in random.

30. A binning along both the rows and columns at the same time by selecting two adjacent rows and two adjacent columns.

31.   The binning as set forth in claim 30 wherein two or more row and column selections are in sequence or random.